FPGA implementation and test of high data rate communication interfaces with a 4-channel high speed ADC card

Internship period: 3 months

Requirements/prior knowledge:

- understanding of digital/logic circuits
- knowledge of hardware description languages (preferably VHDL)
- basic software development methodologies
- C/C++ development experience

Useful knowledge:

- Xilinx FPGAs (Spartan 6 series)
- Xilinx ISE development environment
- High speed (GBit/s) serial interfaces (PCIexpress, SATA, ...)
- device driver development

Description:

Ilmsens has a PCIexpress based interface card containing a 4 channel 14-bit ADC for high speed measurements (up to ~300 MSamples/s).
he ADC is connected to a Xilinx Spartan 6 LXT FPGA, which contains Gigabit transceivers (MGT) that can be used to operate a PCIexpress Gen 1 1x link and an additional Gigabit serial interface to chain multiple cards.
Furthermore, DDR SDRAM based buffer memory and a clock manager are available.

The goal of the internship is to implement the two mentioned GBit speed high bandwidth serial interfaces (PCIex 1 1x, proprietary Card-link) in the FPGA. The PCIex link shall be used to transport acquired ADC data to the host PC. The DDR RAM shall be used as a buffer to accomodate PCIex latencies.
In order to test and benchmark the FPGA implementation, a simple device driver shall be developed (starting form available examples) and a simple application that controls the card(s) and receives the data as fast as possible.
The operating system for the driver/app may be Windows or Linux.

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Provided tools:

Xilinx ISE 14.5 example project for the card (working ADC core) additional Spartan 6 cores (such as DDR memory controller, clock domain management, etc.)
Operating system: Windows 7 x64 or Debian/Ubuntu Linux LTS 16.04
Windows OS: Microsoft SDK/WDM SDK/Visual Studio C++ Express
Linux OS: gcc build environment

Project Goals:

Goal 1: working implementation of above mentioned FPGA cores for PCIex, i.e. ADCs is clocked, acquired data is transferred into DDR buffer, PCIex Gen 1 1x serial interface can be used to transfer data from DDR3 buffer to host PC.

Goal 2: Data transfer at PCIexpress reaches 150 MByte/s (PCI express Gen 1 1x works with 2.5 GBit/s and has raw bandwidth of 250 MByte/s)

Goal 3: MGT up/downlink interface for inter-card communication is working with at least 1GBit/s net speed (125 MByte/s).

If you are interested, please send us an application to recruitment@ilmsens.com.